

Amendments to the Claims:

Claims 1-56 (Previously Cancelled).

57. (Previously Amended): A field effect transistor comprising:  
a pair of source/drain regions having a channel region positioned there  
between; and

a gate positioned operatively proximate the channel region, the gate  
comprising semiconductive material conductively doped with at least one of a p-  
type or n-type conductivity enhancing impurity effective to render the  
semiconductive material electrically conductive, a silicide layer and a conductive  
diffusion barrier layer effective to restrict diffusion of p-type or n-type  
conductivity enhancing impurity, the conductive diffusion barrier layer comprising  
at least two of  $W_xN_y$ ,  $TiO_xN_y$  and  $TiW_xN_y$ .

58. (Previously Amended): The transistor of claim 57 wherein the  
conductive diffusion barrier layer comprises  $W_xN_y$  and  $TiW_xN_y$ .

59. (Previously Amended): The transistor of claim 57 wherein the  
conductive diffusion barrier layer comprises  $TiO_xN_y$  and  $TiW_xN_y$ .

60. (Previously Added): The transistor of claim 57 wherein the  
conductive diffusion barrier layer is formed over the silicide layer.

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D2  
E3 61. (Previously Added): The transistor of claim 57 wherein the silicide layer is formed over the conductive diffusion barrier layer.

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E3 62. (Currently Amended): Integrated circuitry comprising:

a field effect transistor including a gate, a gate dielectric layer, source/drain regions and a channel region; the gate comprising gate semiconductive material conductively doped with a conductivity enhancing impurity of a first type and a conductive diffusion barrier layer effective to restrict diffusion of first or second type conductivity enhancing impurity; and

D3 insulative material received proximate the gate, a contact structure extending through the insulative material to the gate, the contact structure including semiconductive material provided in electrical connection with the gate, the semiconductive material provided through the insulative material being conductively doped with a conductivity enhancing impurity of a second type, the conductive diffusion barrier layer of the gate being provided between the gate semiconductive material and the semiconductive material provided through the insulative material.

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E3 63. (Previously Added): The integrated circuitry of claim 62 wherein the first type is n and the second type is p.

D4 64. (Previously Added): The integrated circuitry of claim 62 wherein the first type is p and the second type is n.

Contd  
D4  
E3

65. (Previously Added): The integrated circuitry of claim 62 wherein the gate also comprises a conductive silicide.

~~D8~~ E3

66. (Previously Amended): The integrated circuitry of claim 65 wherein the silicide and the conductive diffusion barrier layer comprise the same metal.

E3  
D6

67. (Previously Added): The integrated circuitry of claim 62 wherein the semiconductive material within the insulating material contacts the conductive diffusion barrier layer of the gate.

68. (Previously Added): The integrated circuitry of claim 62 wherein the semiconductive material within the insulating material does not contact the conductive diffusion barrier layer of the gate.

69. (Previously Added): The integrated circuitry of claim 62 wherein the gate also comprises a conductive silicide, the semiconductive material within the insulating material contacting the silicide.

70. (Previously Added): The integrated circuitry of claim 62 wherein the conductive diffusion barrier layer is received over the gate semiconductive material, and the semiconductive material within the insulating material is received over the gate.

71. (Previously Added): The integrated circuitry of claim 62 wherein the insulative material comprises an opening within which the semiconductive material therein has been provided, the opening being substantially void of any conductive diffusion barrier layer material.

72. (Previously Amended): The integrated circuitry of claim 62 wherein the conductive diffusion barrier layer comprises a material selected from the group consisting of  $W_xN_y$ ,  $TiO_xN_y$ , and  $TiW_xN_y$ , and mixtures thereof.

73. (Previously Amended): The integrated circuitry of claim 72 wherein the conductive diffusion barrier layer comprises  $W_xN_y$ .

74. (Previously Amended): The integrated circuitry of claim 72 wherein the conductive diffusion barrier layer comprises  $TiO_xN_y$ .

75. (Previously Amended): The integrated circuitry of claim 72 wherein the conductive diffusion barrier layer comprises  $TiW_xN_y$ .

Claims 76 and 77 (Previously Cancelled).

78. (Previously Added): The integrated circuitry of claim 65 wherein the conductive diffusion barrier layer is formed over the silicide layer.

79. (Previously Added): The integrated circuitry of claim 65 wherein the silicide layer is formed over the conductive diffusion barrier layer.

D8  
E3  
80. (Previously Added): The integrated circuitry of claim 62 wherein the gate includes opposing sidewalls in at least one cross section, the contact structure have opposing sidewalls in the one cross section, at least one of the contact structure sidewalls not aligning with either of the opposing sidewalls of the gate in the one cross section.

81. (Previously Added): The integrated circuitry of claim 62 wherein the gate includes opposing sidewalls in at least one cross section, the contact structure have opposing sidewalls in the one cross section, neither of the contact structure sidewalls aligning with either of the opposing sidewalls of the gate in the one cross section.

82. (Previously Added): The integrated circuitry of claim 62 wherein the conductive diffusion barrier layer comprising at least two of  $W_xN_y$ ,  $TiO_xN_y$  and  $TiW_xN_y$ .

83. (Previously Added): The integrated circuitry of claim 82 wherein the conductive diffusion barrier layer comprises  $W_xN_y$  and  $TiW_xN_y$ .

84. (Previously Added): The integrated circuitry of claim 82 wherein the conductive diffusion barrier layer comprises  $TiO_xN_y$  and  $TiW_xN_y$ .

85. (Previously Added): The integrated circuitry of claim 62 wherein the gate is defined by a single conductive region consisting of a) the conductively doped semiconductive material of the first type, and b) the conductive diffusion barrier layer.

86. (Previously Added): The integrated circuitry of claim 85 wherein the conductive diffusion barrier layer comprising at least two of  $W_xN_y$ ,  $TiO_xN_y$  and  $TiW_xN_y$ .

87. (Previously Added): The integrated circuitry of claim 85 wherein the conductive diffusion barrier layer comprises  $W_xN_y$  and  $TiW_xN_y$ .

88. (Previously Added): The integrated circuitry of claim 85 wherein the conductive diffusion barrier layer comprises  $TiO_xN_y$  and  $TiW_xN_y$ .

Contd  
D5  
E3

89. (Previously Added): The integrated circuitry of claim 62 wherein the gate is defined by a single conductive region consisting of a) the conductively doped semiconductive material of the first type, b) the conductive diffusion barrier layer; and c) a conductive silicide.

90. (Previously Added): The integrated circuitry of claim 89 wherein the conductive diffusion barrier layer comprising at least two of  $W_xN_y$ ,  $TiO_xN_y$  and  $TiW_xN_y$ .

91. (Previously Added): The integrated circuitry of claim 89 wherein the conductive diffusion barrier layer comprises  $W_xN_y$  and  $TiW_xN_y$ .

92. (Previously Added): The integrated circuitry of claim 89 wherein the conductive diffusion barrier layer comprises  $TiO_xN_y$  and  $TiW_xN_y$ .

93. (Added): The field effect transistor of claim 57 wherein the conductive diffusion barrier layer comprises  $W_xN_y$  and  $TiO_xN_y$ .

94. (Added): The integrated circuitry of claim 82 wherein the conductive diffusion barrier layer comprising at  $W_xN_y$  and  $TiO_xN_y$ .

95. (Added): The integrated circuitry of claim 86 wherein the conductive diffusion barrier layer comprises  $W_xN_y$  and  $TiO_xN_y$ .

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P  
E3

96. (Added): The integrated circuitry of claim 90 wherein the  
conductive diffusion barrier layer comprises  $W_xN_y$  and  $TiO_xN_y$ .

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